What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A priority encoding circuit comprising:

input lines, each providing an input signal; output lines, each providing a priority signal indicating whether a respective input signal is asserted and has priority, at most one of the priority signals being asserted at a time;

first tree-like circuitry that responds to the input signals, providing subset signals; the subset signals each indicating whether any of a subset of the input signals is asserted; and

second tree-like circuitry that responds to the subset signals, providing the priority signals on the output lines.

2. The circuit of claim 1 in which the first tree-like circuitry includes static logic.

3. The circuit of claim 1 in which the second tree-like circuitry includes dynamic logic.

4. The circuit of claim 1 in which the first tree-like circuitry provides power-of-two subset signals, each indicating whether any of a power-of-two subset of the input signals is asserted.

5. The circuit of claim 1 in which the second tree-like circuitry provides each priority signal in response to a non-redundant group of the subset signals.

6. The circuit of claim 1 in which the second tree-like circuitry provides each input signal's respective priority signal independently of any other input signal's priority signal.

7. A priority encoding circuit comprising:

M input lines, each providing an input signal; M output lines, each providing a priority signal indicating whether a respective input signal is asserted and has priority, at most one of the priority signals being asserted at a time; M being equal to 2^N; and

first circuitry that responds to the M input signals, providing subset signals, each indicating whether any of a respective subset of the input signals is asserted; the subsets including, for n=0 to (N—1), $2^{N-(n+1)}$ subsets of 2^n input signals; and

second circuitry that responds to the M input signals and the subset signals, providing the priority signals on the output lines; each of the priority signals depending on no more than N of the subset signals.

8. The circuit of claim 7 in which M is equal to sixteen and N is equal to four.

9. The circuit of claim 7 in which the first circuitry includes static logic.

10. The circuit of claim 7 in which the second circuitry includes dynamic logic.

11. A priority encoding circuit comprising:

sixteen input lines, each providing an input signal; sixteen output lines, each providing a priority signal indicating whether a respective input signal is asserted and has priority, at most one of the priority signals being asserted at a time;

first hierarchical circuitry that responds to the input signals, the first hierarchical circuitry having a first level that provides eight one-line signals, a second level that provides four two-line signals, a third level that provides two four-line signals, and a fourth level that provides one eight-line signal; and

second hierarchical circuitry that responds to the input signals, the one-line signals, the two-line signals, the four-line signals, and the eight-line signal, providing the priority signals on the output lines; the second hierarchical circuitry having switching elements connected in series to control each output line; the switching elements being in levels, including:

a first level at which, for i=1 through 16, a switching element in series with an ith output line is controlled by an input signal from an ith input line;

a second level at which, for every other value of i, a switching element in series with the ith output line is controlled by an (i—1)th one-line signal;

a third level at which, for j=1 through 4, a switching element in series with ($4j$)th and ($4j$—1)th output lines is controlled by a jth two-line signal;

a fourth level at which, for k=1 through 2, a switching element in series with ($8k$)th through ($8k$—3)th output lines is controlled by a kth four-line signal; and

a fifth level at which a switching element in series with ninth through sixteenth output lines is controlled by the eight-line signal.

12. The circuit of claim 11 in which the switching elements are transistors.

13. A priority encoding circuit comprising:

input lines, each providing an input signal; output lines, each providing a priority signal indicating whether a respective input signal is asserted and has priority, at most one of the priority signals being asserted at a time;

first circuitry that responds to the input signals, providing subset signals; each subset signal indicating whether any of a power-of-two subset of the input signals is asserted; and

second circuitry that responds to the subset signals, providing the priority signals on the output lines; the second circuitry providing each priority signal in response to a non-redundant group of the subset signals.

14. The circuit of claim 13, with sixteen of the input lines; the subset signals including four two-line signals, two four-line signals, and one eight-line signal.

15. The circuit of claim 13 in which the second circuitry includes, for each output line, a respective series of switching elements in series that control the output line's priority signal; each output line's series of switching elements including, for each of its priority signal's non-redundant group of subset signals, a switching element controlled by the subset signal.

16. A priority encoding circuit comprising:

input lines; each providing an input signal; output lines, each providing a priority signal indicating whether a respective input signal is asserted and has priority, at most one of the priority signals being asserted at a time;

first circuitry that responds to the input signals, providing subset signals; each subset signal indicating whether any of a subset of the input signals is asserted; and

second circuitry that responds to the subset signals, providing the priority signals on the output lines; the second circuitry providing each priority signal in response to a group of the subset signals; the second circuitry providing each input signal's priority signal independently of any other input signal's priority signal.

17. The circuit of claim 16 in which the second circuitry includes, for each output line, a respective series of switching elements in series that control the output line's priority signal; each output line's series of switching elements including, for each of its priority signal's group of subset signals, a switching element controlled by the subset signal; none of the switching elements being controlled by any other output line's priority signal.

18. A priority encoding circuit comprising:

input lines, each providing an input signal; output lines, each providing a priority signal indicating whether a respective input signal is asserted and has priority, at most one of the priority signals being asserted at a time;

static circuitry that responds to the input signals, providing subset signals; each subset signal indicating whether any of a subset of the input signals is asserted; and

dynamic circuitry that responds to the subset signals, providing the priority signals on the output lines.

19. The circuit of claim 18 in which the static circuitry includes NOR and NAND gates.

20. The circuit of claim 18 in which the dynamic circuitry includes NMOS devices.

21. The circuit of claim 18 in which the dynamic circuitry includes, for each output line, one or more respective switching elements in series to control the output line, the switching elements forming a dynamic AND gate, the output line's priority signal being asserted only when all the respective switching elements are on.

22. The circuit of claim 18 in which the dynamic circuitry includes transistors and, for a set of the transistors, precharging circuitry for precharging the transistors.

23. A priority encoder comprising:

lower level priority encoding circuits, each including:

input lines, each providing an input signal;

first tree-like circuitry that responds to the input signals, providing a set of subset signals, each indicating whether any of a subset of the input signals is asserted; the subset signals including an overall signal indicating whether any of the input signals is asserted; and

second tree-like circuitry that responds to the subset signals, providing lower level priority signals, each lower level priority signal indicating whether a respective input signal is asserted and has priority, at most one of the lower level priority signals being asserted at a time;

lower output lines that provide the lower level priority signals from one of the lower level priority encoders at a time; and

an upper level priority encoding circuit including:

upper output lines, each providing an upper level priority signal indicating whether a respective overall signal is asserted and has priority, at most one of the upper level priority signals being asserted at a time; and

prioritizing circuitry that responds to the overall signals, providing the upper level priority signals on the upper output lines.

24. The priority encoder of claim 23 in which the first tree-like circuitry includes static logic, the second tree-like circuitry includes dynamic logic, and the prioritizing circuitry includes static logic.

25. The priority encoder of claim 23, further including lower level select circuitry that responds to the upper level priority signals, selecting one of the lower level priority encoding circuits to provide its lower level priority signals on the lower output lines.

26. A circuit comprising:

lower level priority encoding circuits, each including:

input lines, each providing an input signal; and

lower prioritizing circuitry that responds to the input signals, providing lower level priority signals and a overall signal; each lower level priority signal indicating whether a respective input signal is asserted and has priority, at most one of the lower level priority signals being asserted at a time; the overall signal indicating whether any of the input signals is asserted; and

upper level priority encoding circuitry including:

output lines, each providing an upper level priority signal indicating whether a respective overall signal is asserted and has priority, at most one of the upper level priority signals being asserted at a time; and

prioritizing circuitry that responds to the overall signals, providing upper level priority signals, each upper level priority signal indicating whether a respective overall signal is asserted and has priority, at most one of the upper level priority signals being asserted at a time.

27. A method of priority encoding, comprising:

in response to input signals, obtaining subset signals, each subset signal indicating whether any of a power-of-two subset of the input signals is asserted; and

in response to the subset signals, providing priority signals, each priority signal indicating whether a respective input signal is asserted and has priority, at most one of the

priority signals being asserted at a time; each priority signal being provided in response to a non-redundant group of the subset signals.

28. A method of priority encoding, comprising:

in response to input signals, obtaining subset signals, each subset signal indicating whether any of a subset of the input signals is asserted; and

in response to the subset signals, providing priority signals, each priority signal indicating whether a respective input signal is asserted and has priority, at most one of the priority signals being asserted at a time; each input signal's priority signal being provided in response to a group of the subset signals; each input signal's priority signal being obtained independently of any other input signal's priority signal.

29. A method of priority encoding, comprising:

in response to M input signals, where M is equal to 2^N, obtaining subset signals, each subset signal indicating whether any of a subset of the input signals is asserted; the subsets including, for n=0 to (N—1), $2^{N-(n+1)}$ subsets of 2^n input signals; and

in response to the input signals and the subset signals, providing priority signals on M output lines; each output line's priority signal indicating whether a respective input signal is asserted and has priority, at most one of the priority signals being asserted at a time; each of the priority signals depending on no more than N of the subset signals.

30. The method of claim 29 in which M is sixteen and N is four.

31. A method of priority encoding, comprising:

receiving input signals on M groups of M input lines each, M being equal to 2^N;

in response to the input signals on each group of input lines:

obtaining subset signals, each subset signal indicating whether any of a subset of the group of input signals is asserted; the subsets including, for n=0 to (N—1), $2^{N-(n+1)}$ subsets of 2^n input signals; and

in response to the input signals on the input lines in the group and the subset signals, providing group priority signals and a group overall signal; each group priority signal indicating whether a respective input signal in the group is asserted and has priority, at most one of the group priority signals being asserted; each of the group priority signals depending on no more than N of the subset signals; the group overall signal indicating whether any of the group priority signals is asserted; and

in response to the group overall signals of the M groups, providing a priority group overall signal for each group indicating whether the group's overall signal is asserted and has priority, at most one of the priority group overall signals being asserted.

32. The method of claim 31 in which M is sixteen and N is four.

33. An integrated circuit comprising:

a substrate with a surface;

priority encoder circuitry that responds to input signals, providing priority signals indicating an input signal that is asserted and has priority; the priority encoder circuitry including:

first circuitry that responds to a group of the input signals, providing subset signals; the subset signals each indicating whether any of a subset of the group of input signals is asserted; and

second circuitry that responds to the subset signals, providing the priority signals.

34. The integrated circuit of claim 33 in which each subset signal indicates whether any of a power-of-two subset of the input signals is asserted.

35. The integrated circuit of claim 33 in which the second circuitry provides a respective one of the priority signals for each of the input signals, the second circuitry providing each input signal's priority signal in response to a non-redundant group of the subset signals.

36. A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including:

priority encoder circuitry that responds to input signals, providing priority signals indicating an input signal that is asserted and has priority; the priority encoder asserting at most one of the priority signals at a time; the priority encoder circuitry including:

first tree-like circuitry that responds to the input signals, providing subset signals; the subset signals each indicating whether any of a subset of the input signals is asserted; and

second tree-like circuitry that responds to the subset signals, providing the priority signals.

37. A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including:

priority encoder circuitry that responds to input signals, providing priority signals indicating an input signal that is asserted and has priority; the priority encoder asserting at most one of the priority signals at a time; the priority encoder circuitry including:

first circuitry that responds to the input signals, providing subset signals; the subset signals each indicating whether any of a power-of-two subset of the input signals is asserted; and

second circuitry that responds to the subset signals, providing the priority signals; the second circuitry providing each priority signal in response to a non-redundant group of the subset signals.

38. A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including:

priority encoder circuitry that responds to input signals, providing priority signals indicating an input signal that is asserted and has priority; the priority encoder asserting at most one of the priority signals at a time; the priority encoder circuitry including:

first circuitry that responds to the input signals, providing subset signals; the subset signals each indicating whether any of a subset of the input signals is asserted; and

second circuitry that responds to the subset signals, providing the priority signals; the second circuitry providing each priority signal in response to a group of the subset

signals; the second circuitry providing each input signal's priority signal independently of any other input signal's priority signal.

39. A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including:

priority encoder circuitry that responds to input signals, providing priority signals indicating an input signal that is asserted and has priority; the priority encoder asserting at most one of the priority signals at a time; the priority encoder circuitry including:

static circuitry that responds to the input signals, providing subset signals; the subset signals each indicating whether any of a subset of the input signals is asserted; and

dynamic circuitry that responds to the subset signals, providing the priority signals.

40. A system comprising:

a processor;

a CAM component connected for access by the processor, the CAM component including:

priority encoder circuitry that responds to input signals, providing priority signals indicating an input signal that is asserted and has priority; the priority encoder circuitry including:

first circuitry that responds to a group of the input signals, providing subset signals; the subset signals each indicating whether any of a subset of the group of input signals is asserted; and

second circuitry that responds to the subset signals, providing the priority signals.

41. A router comprising:

input lines that receive data transmissions;

output lines that retransmit data transmissions received on the input lines;

CAM circuitry that provides information used to retransmit data transmissions on the output lines, the CAM circuitry comprising:

priority encoder circuitry that responds to match signals, providing priority signals indicating a match signal that is asserted and has priority; the priority encoder asserting at most one of the priority signals at a time; the priority encoder circuitry including:

first tree-like circuitry that responds to the match signals, providing subset signals; the subset signals each indicating whether any of a subset of the match signals is asserted; and

second tree-like circuitry that responds to the subset signals, providing the priority signals.

42. A router comprising:

input lines that receive data transmissions;

output lines that retransmit data transmissions received on the input lines;

CAM circuitry that provides information used to retransmit data transmissions on the output lines, the CAM circuitry comprising:

priority encoder circuitry that responds to match signals, providing priority signals indicating a match signal that is asserted and has priority; the priority encoder asserting at most one of the priority signals at a time; the priority encoder circuitry including:

first circuitry that responds to the match signals, providing subset signals; the subset signals each indicating whether any of a power-of-two subset of the match signals is asserted; and

second circuitry that responds to the subset signals, providing the priority signals; the second circuitry providing each priority signal in response to a non-redundant group of the subset signals.

43. A router comprising:

input lines that receive data transmissions;

output lines that retransmit data transmissions received on the input lines;

CAM circuitry that provides information used to retransmit data transmissions on the output lines, the CAM circuitry comprising:

priority encoder circuitry that responds to match signals, providing priority signals indicating a match signal that is asserted and has priority; the priority encoder asserting at most one of the priority signals at a time; the priority encoder circuitry including:

first circuitry that responds to the match signals, providing subset signals; the subset signals each indicating whether any of a subset of the match signals is asserted; and

second circuitry that responds to the subset signals, providing the priority signals; the second circuitry providing each priority signal in response to a group of the subset signals; the second circuitry providing each match signal's priority signal independently of any other match signal's priority signal.

44. A router comprising:

input lines that receive data transmissions;

output lines that retransmit data transmissions received on the input lines;

CAM circuitry that provides information used to retransmit data transmissions on the output lines, the CAM circuitry comprising:

priority encoder circuitry that responds to match signals, providing priority signals indicating a match signal that is asserted and has priority; the priority encoder asserting at most one of the priority signals at a time; the priority encoder circuitry including:

static circuitry that responds to the match signals, providing subset signals; the subset signals each indicating whether any of a subset of the match signals is asserted; and

dynamic circuitry that responds to the subset signals, providing the priority signals.